UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/668,089	09/23/2003	Shino Matsubara	027260-672	1277

21839 7590 09/06/2005

BUCHANAN INGERSOLL PC
(INCLUDING BURNS, DOANE, SWECKER & MATHIS)
POST OFFICE BOX 1404
ALEXANDRIA, VA 22313-1404

EXAMINER	
TO, TUYEN P	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 09/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/668,089	MATSUBARA, SHINO	
	Examiner	Art Unit	
	Tuyen To	2825	77

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *09/23/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is a response to the communication filed on 09/23/2003. Claims 1-3 are pending.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) The invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-3 are rejected under 35 U.S.C. 102(e) as being anticipated by Fitzhenry et al. (Fitzhenry) (U.S. Patent No. 6766503).

Referring to claim 1, Fitzhenry discloses a layout design apparatus for carrying out layout design of a semiconductor integrated circuit (col. 1, lines 13-16), said layout design apparatus comprising:

a region decision section (Fig. 5, step 502) for determining, in the semiconductor integrated circuit including a first circuit and a second circuit, a first circuit region to be assigned to the first circuit and a second circuit region to be assigned to the second circuit (col. 3, lines 53-59);

an initial layout section for carrying out placement and routing using a netlist of the entire semiconductor integrated circuit (Fig. 1, element 102; col. 4, lines 58+; col. 5, lines 1-4) such that a layout of the first circuit whose wiring consists of n wiring layers is formed in the first circuit region, where n is an integer equal to or greater than two (Fig. 2, element B1; col. 6, lines 28-37), and that a layout of the second circuit, which has wiring consisting of (n-m) wiring layers and is connected to the layout of the first circuit (Fig. 2, HR and TL blocks), is formed in the second circuit region, where m is a positive integer less than n (Fig. 2); and

a layout modifying section for carrying out placement and routing using a netlist of a third circuit (Fig. 3, modified circuit) to form a layout of the third circuit (Fig. 1; col. 5, lines 2-4 and lines 9-29) such that wiring of the third circuit consists of the (n-m) wiring layers constituting the wiring of the second circuit (Fig. 2, HR and TL blocks), and for replacing the layout of the second circuit formed by said initial layout section by the layout of the third circuit (col. 5, lines 50-53).

Referring to claim 2, Fitzhenry discloses the layout design apparatus according to claim 1, wherein said layout modifying section comprises:

a netlist creating section for creating the netlist of the third circuit (col. Fig. 1, col. 4, lines 58+; col. 6, lines 1-7);

a placement and routing section for carrying out the placement and routing using the netlist of the third circuit (Fig. 5; col. 8, lines 3-11) to form the layout of the third circuit such that the wiring of the third circuit consists of the (n-m) wiring layers constituting the wiring of the second circuit (Fig. 2; col. 6, lines 28-37); and

a connecting section for replacing the layout of the second circuit formed by said initial layout section by the layout of the third circuit, and for connecting the layout of the third circuit to the layout of the first circuit (Fig. 6; col. 8, lines 40-48).

Referring to claim 3, Fitzhenry discloses the layout design apparatus according to claim 1, wherein the layout of the third circuit is connectable to the layout of the first circuit using the wiring connecting the layout of the second circuit to the layout of the first circuit (Fig. 2-3; col. 3, lines 13-23).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuyen To whose telephone number is 571-272-8319. The examiner can normally be reached on Monday to Friday from 9:00am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tuyen To
Patent Examiner Tuyen To

Thuan
THUAN - DO
Primary examiner.
08/29/2005